

A 22mW Bluetooth RF Transceiver with Direct RF Modulation and On-chip Filtering

Norm Filiol, Neil Birkett, James Cherry, Florinel Balteanu,
Christian Cojocaru, Ardeshir Namdar, Tolga Pamir, Kashif Sheikh,
Gilles Glandon, Daniel Payer, Ashok Swaminathan, Robert Forbes,
¹Thomas Riley, S.M. Alinoor, Edward Mac Robbie, Mark Cloutier,
²Spyros Pipilos, ²Theo Varelas

Conexant Systems Inc., Ottawa, Canada*

¹University of Oulu, Oulu, Finland

²Theta Microelectronics, Athens, Greece

Outline

- Introduction
- Transceiver architecture
- Transmitter
- Receiver
- Measurement results
- Conclusions

Bluetooth

- Cable replacement/ad hoc networking
- 2.4GHz – 2.5GHz ISM Band
- 79 channels with 1MHz spacing
- Frequency hopping at 1600hops/s
- 1Mb/s 2-level GFSK modulation
- Modulation index = 0.28 - 0.35
- Transmit power
 - +0dBm for 10m (**This work**)
 - +20dBm for 100m (Power control required)

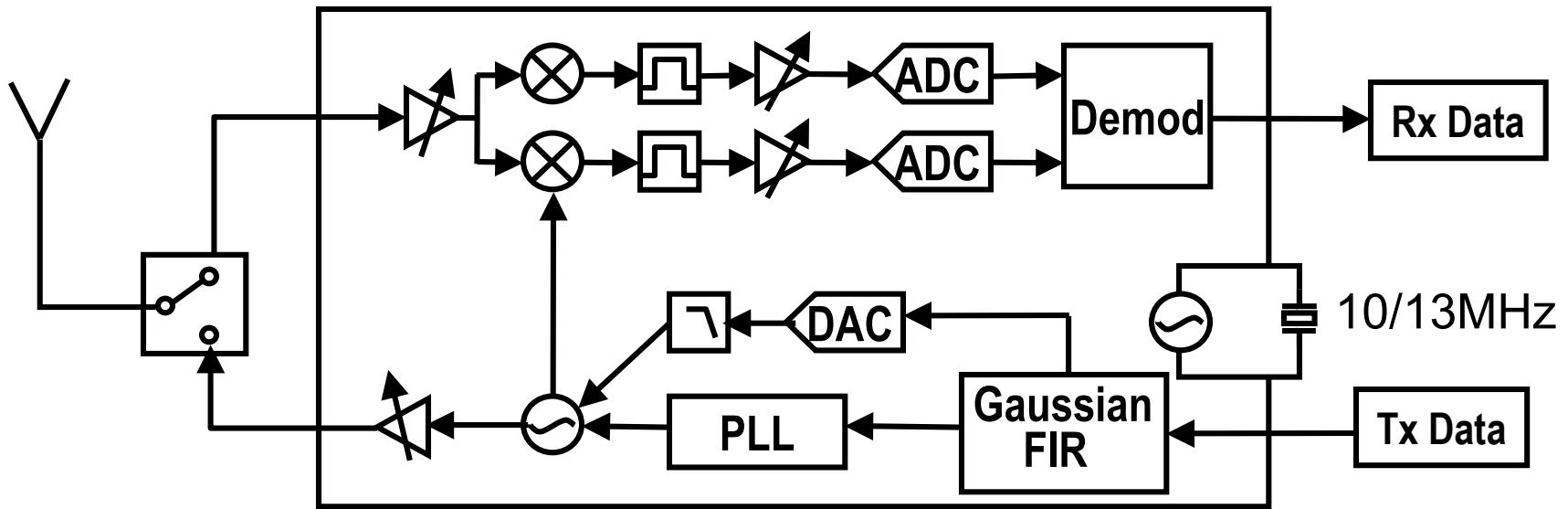
Bluetooth Applications

- Highly mobile devices are the key
 - Wireless headsets
 - Handsets
 - Personal digital assistants
 - Digital cameras
- **Lower power = longer battery life**

Goals

- Bluetooth for portable applications
 - Average power consumption 22mW @+2dBm
- Full integration
 - PLL, VCO, PA, IF filters, demodulator
- How was this achieved?
 - Careful architecture choice (direct modulation,low IF)
 - 1.6V - 3.0V operation
 - 0.5μm SiGe BiCMOS process

Transceiver Block Diagram



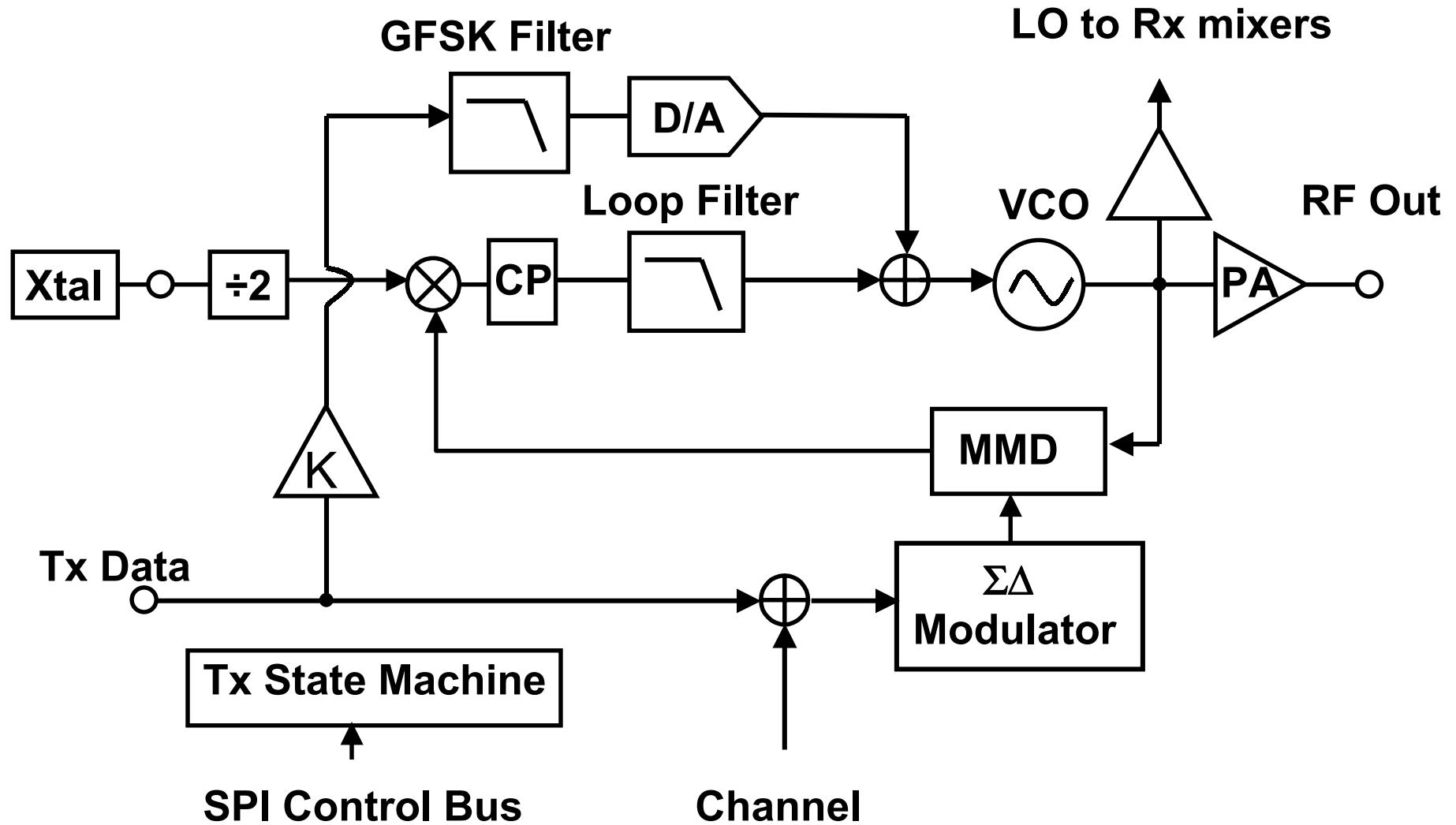
•2-level GFSK Transmitter at 1Mb/s

- **$\Delta\Sigma$ controlled fractional-N synthesizer**
- **Direct two-point modulation at RF**
- **Modulation deviation calibration**

•Receiver

- **Low IF 7-pole image reject complex IF filtering**
- **Automatic IF filter tuning**
- **Distributed feedforward AGC**
- **Complex PLL based digital demodulator**

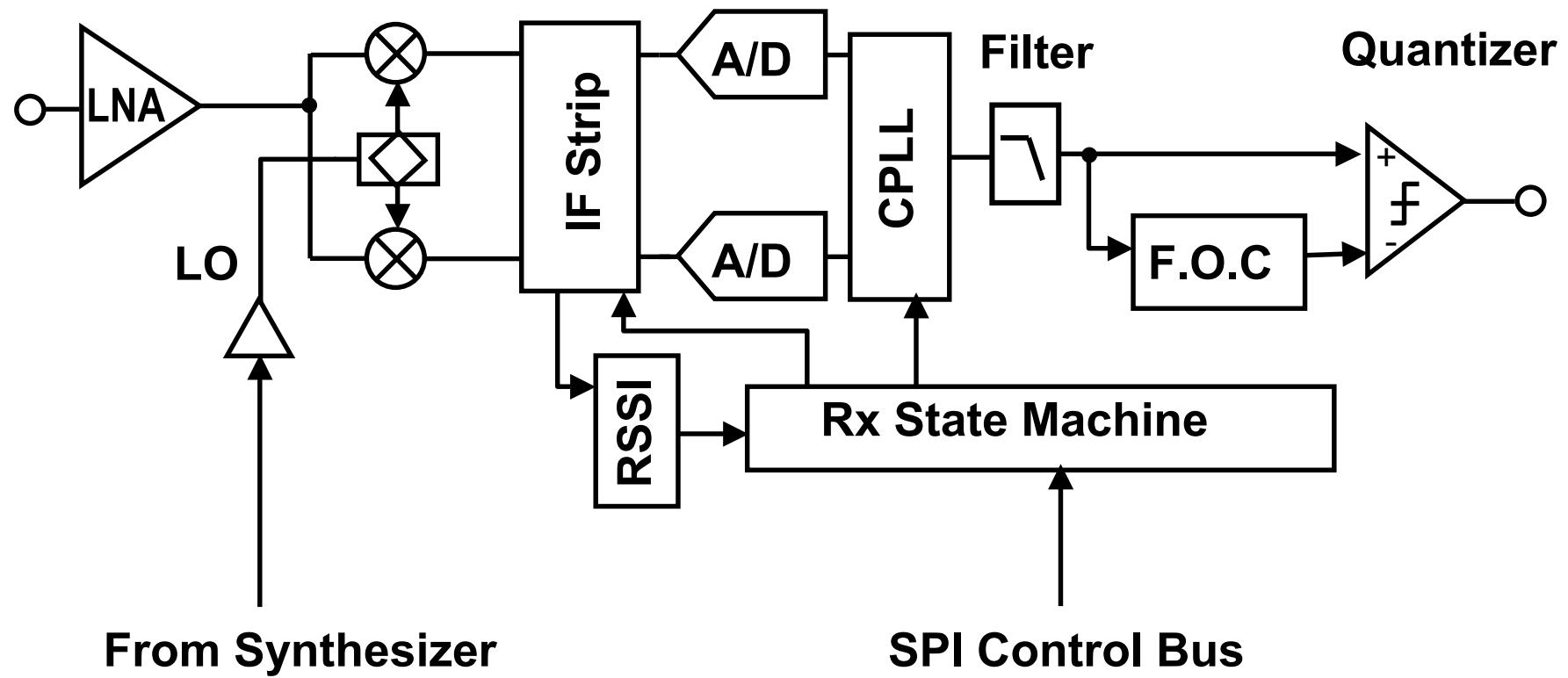
Transmitter Block Diagram



Transmitter Advantages

- Lower parts count than I/Q upconversion
 - No direct digital synthesizer required
 - No I/Q upconversion mixers required
 - No sideband rejection required
- Direct closed loop modulation
 - Carrier locked during transmission
- Fractional-N allows lower division ratios

Receiver Block Diagram

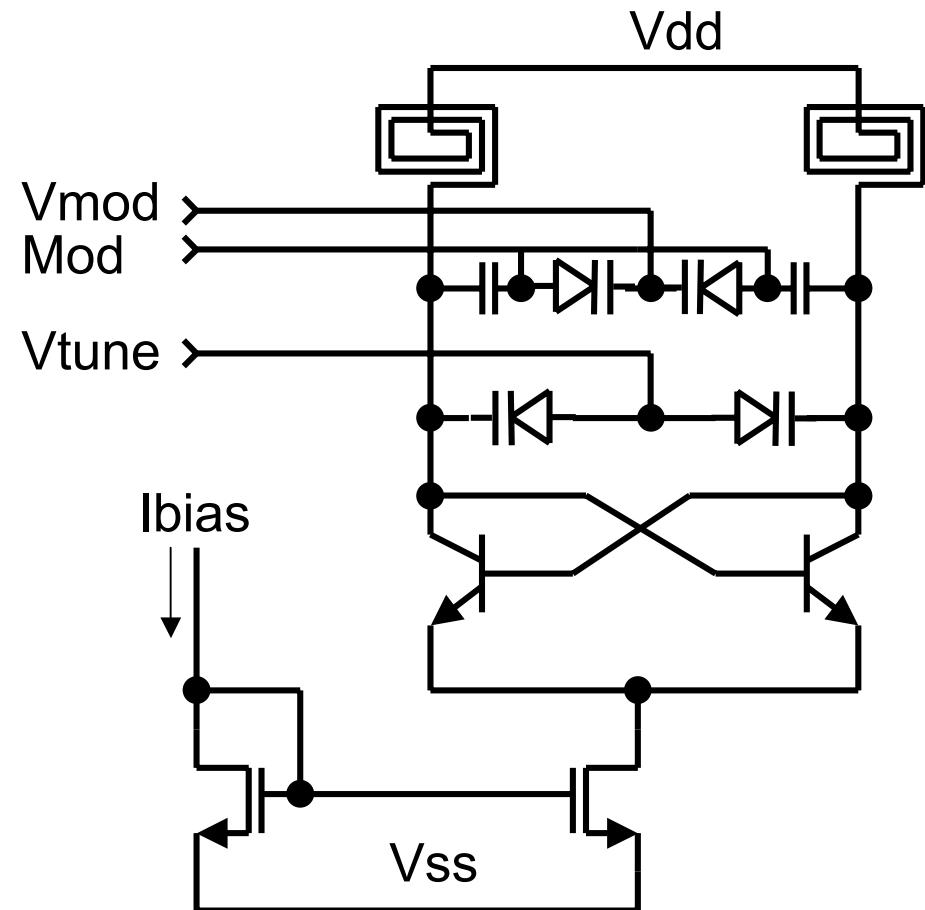


Receiver Advantages

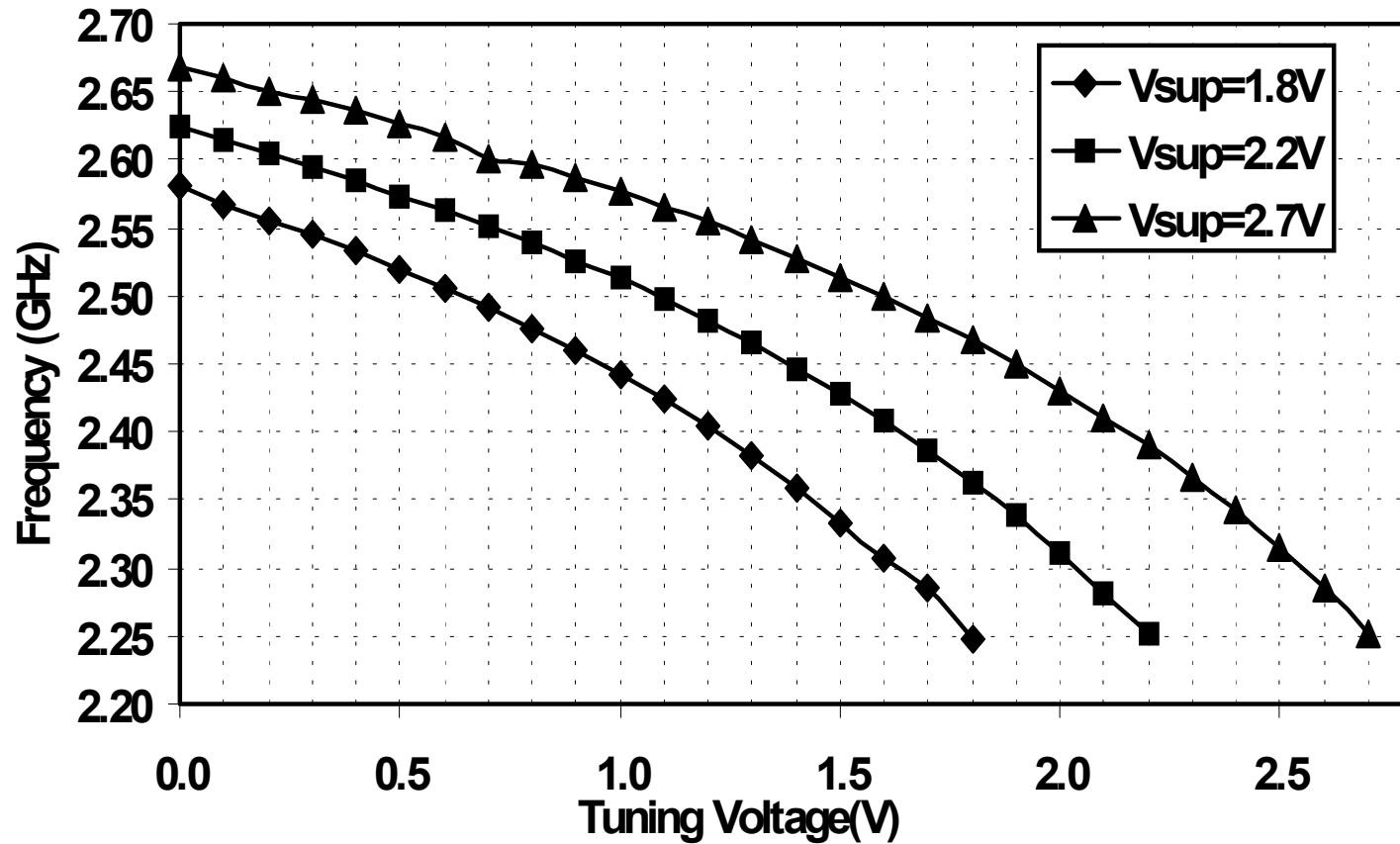
- Low IF uses complex filters for image rejection and pole count reduction
- Dynamic DC offsets are mitigated
- Distributed feedforward AGC is stable
- Complex domain provides four phases for fast AGC response
- No drivers required for off chip filters
- Complex PLL demodulator requires no external components

2.5GHz VCO with Modulation Port

- On chip spiral inductors
 $Q=7$
- 1MHz/V modulation port
- Phase noise -110dBc/Hz
@ 1MHz
- Power 1mA @ 1.6V



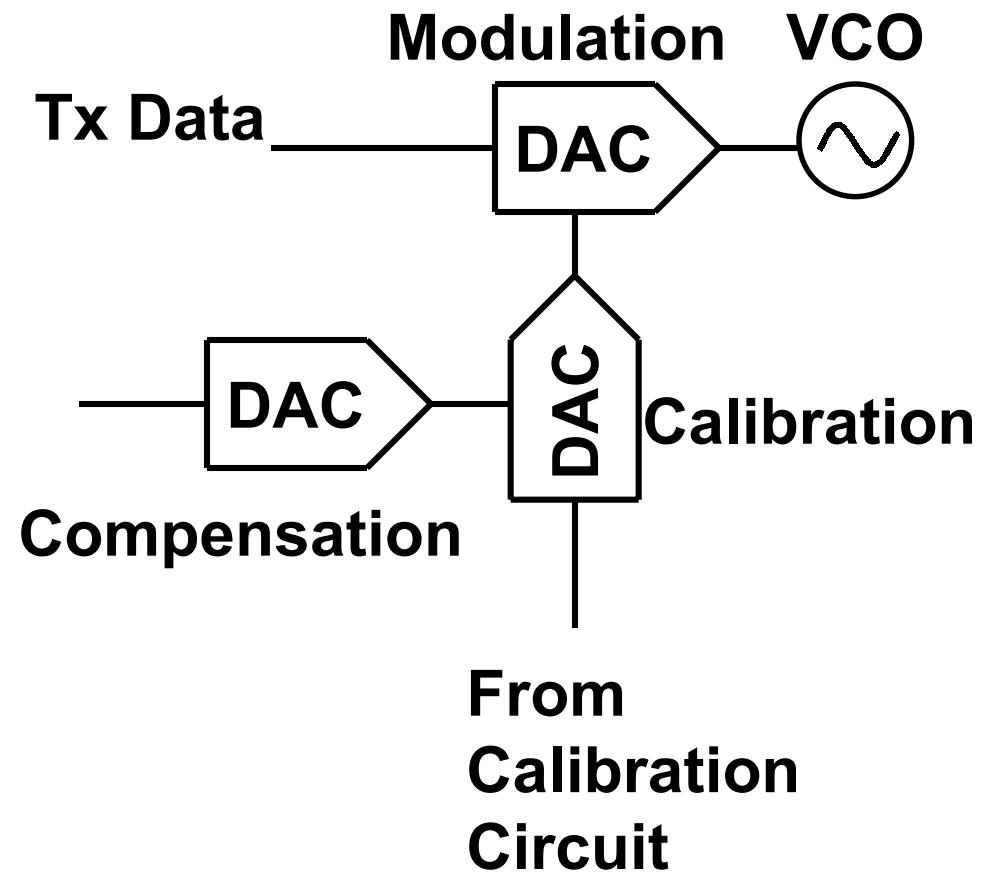
Measured VCO Tuning Curve



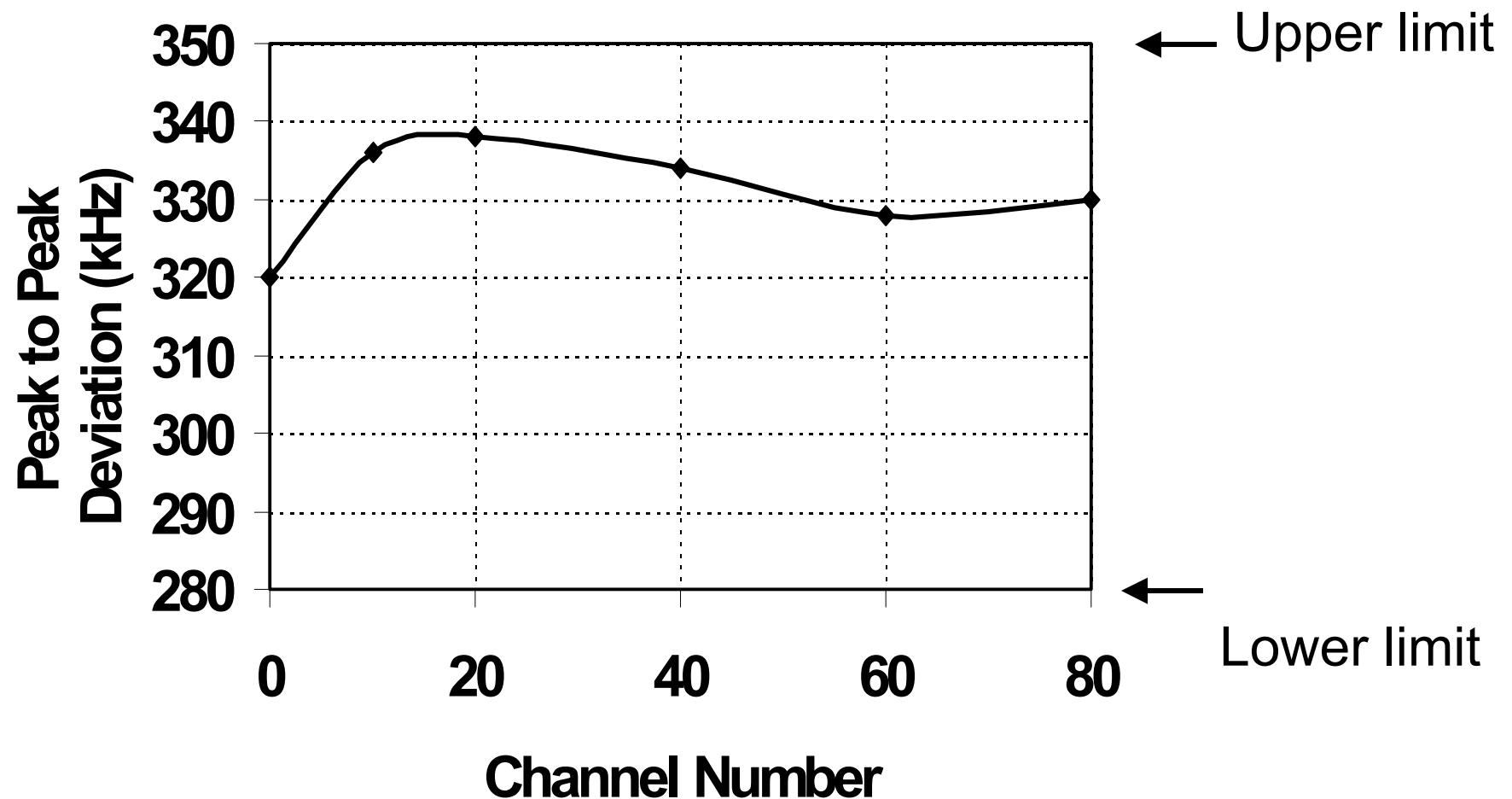
$$\Delta f = 330\text{MHz} @ 1.8V$$

Modulation Deviation Setting

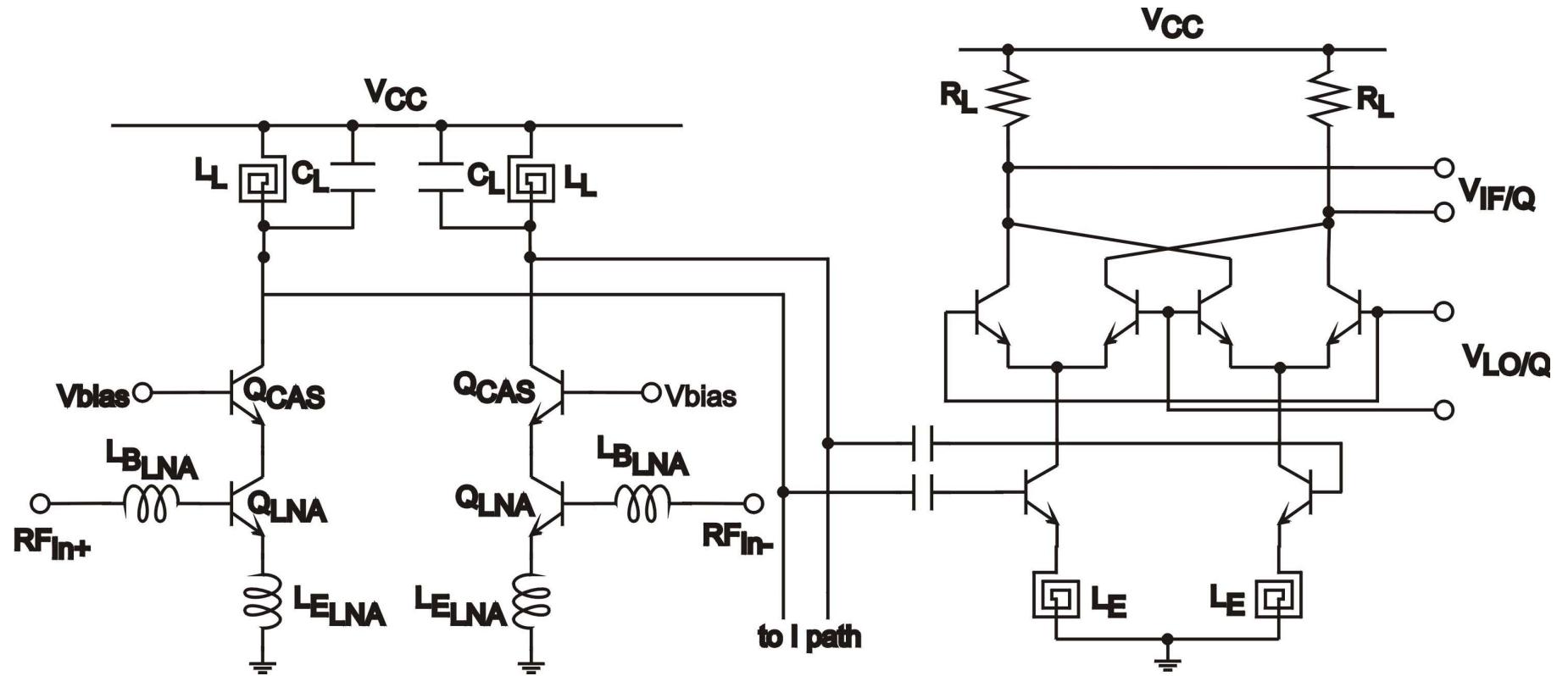
- Calibration circuit sets fullscale range of modulation DAC
- Compensation DAC is for fine tuning of the deviation
- 6% Deviation variation across band



Modulation Deviation Variation Over Transmit Band

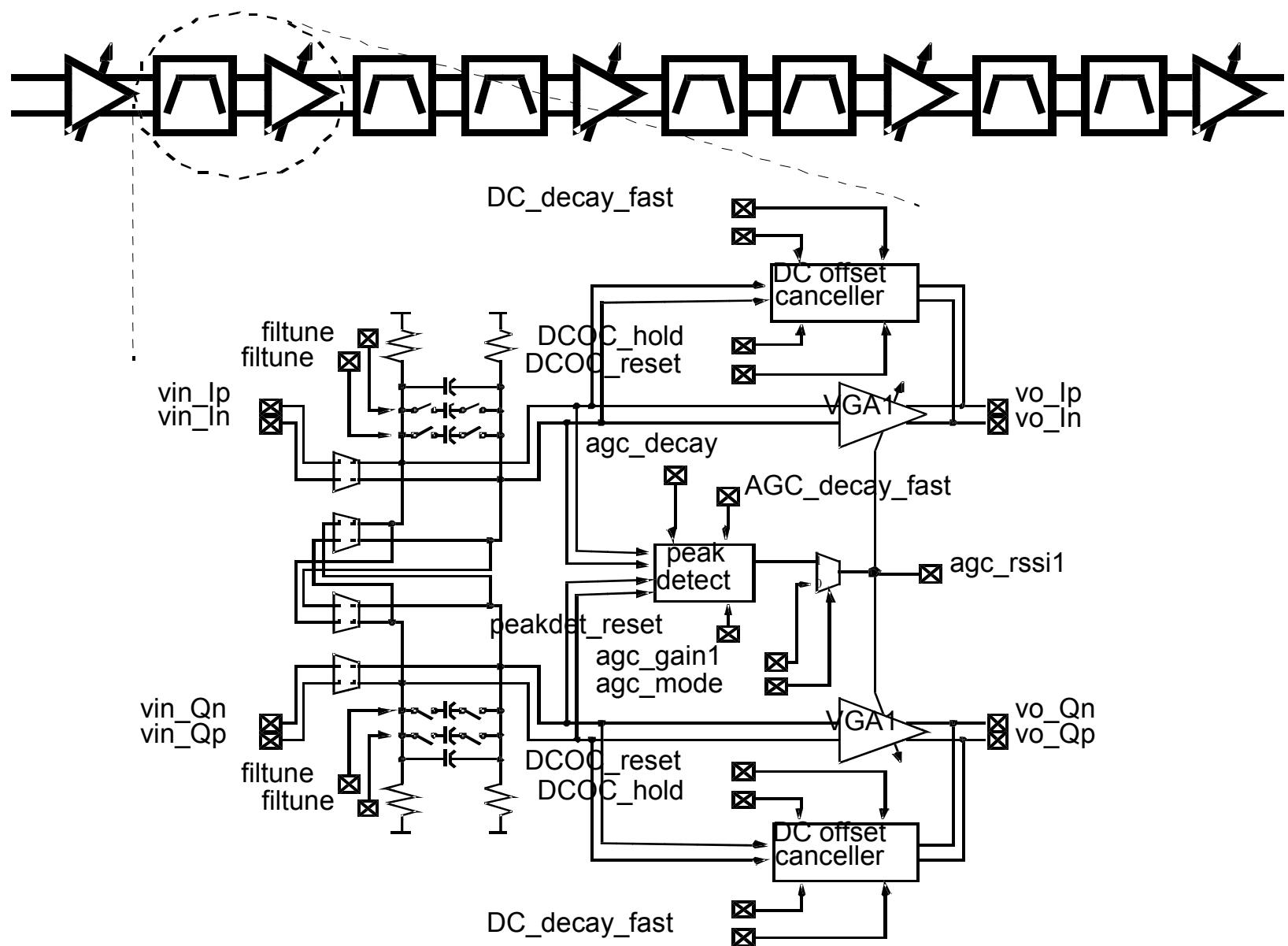


RF Front-end



- Small signal gain = 14dB
- Noise figure = 6.5dB
- IP3 = -15dBm
- Image rejection > 21dB
- Power = 4.5mA @ 1.8V
- 1V operation possible

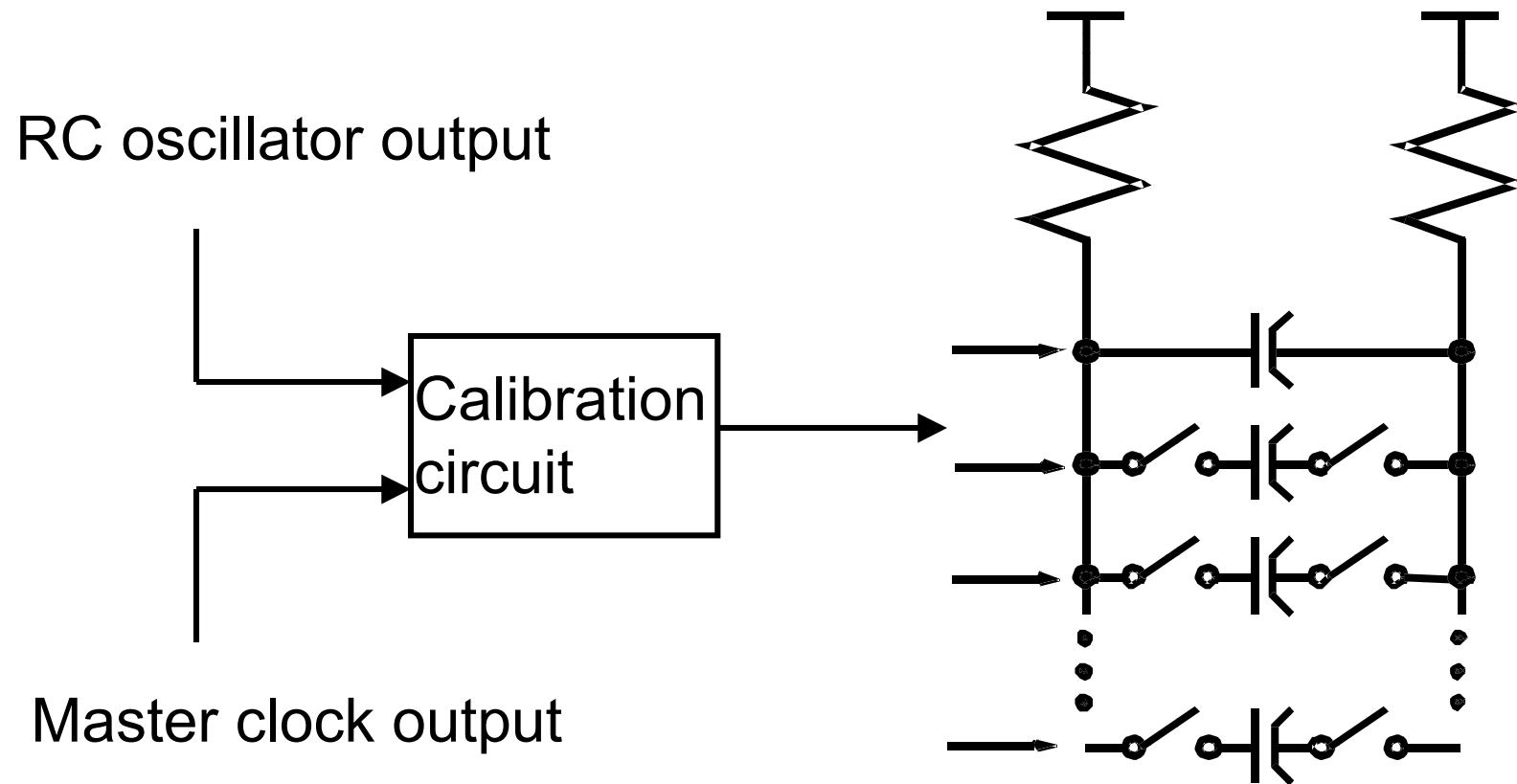
IF Filters



IF Filter

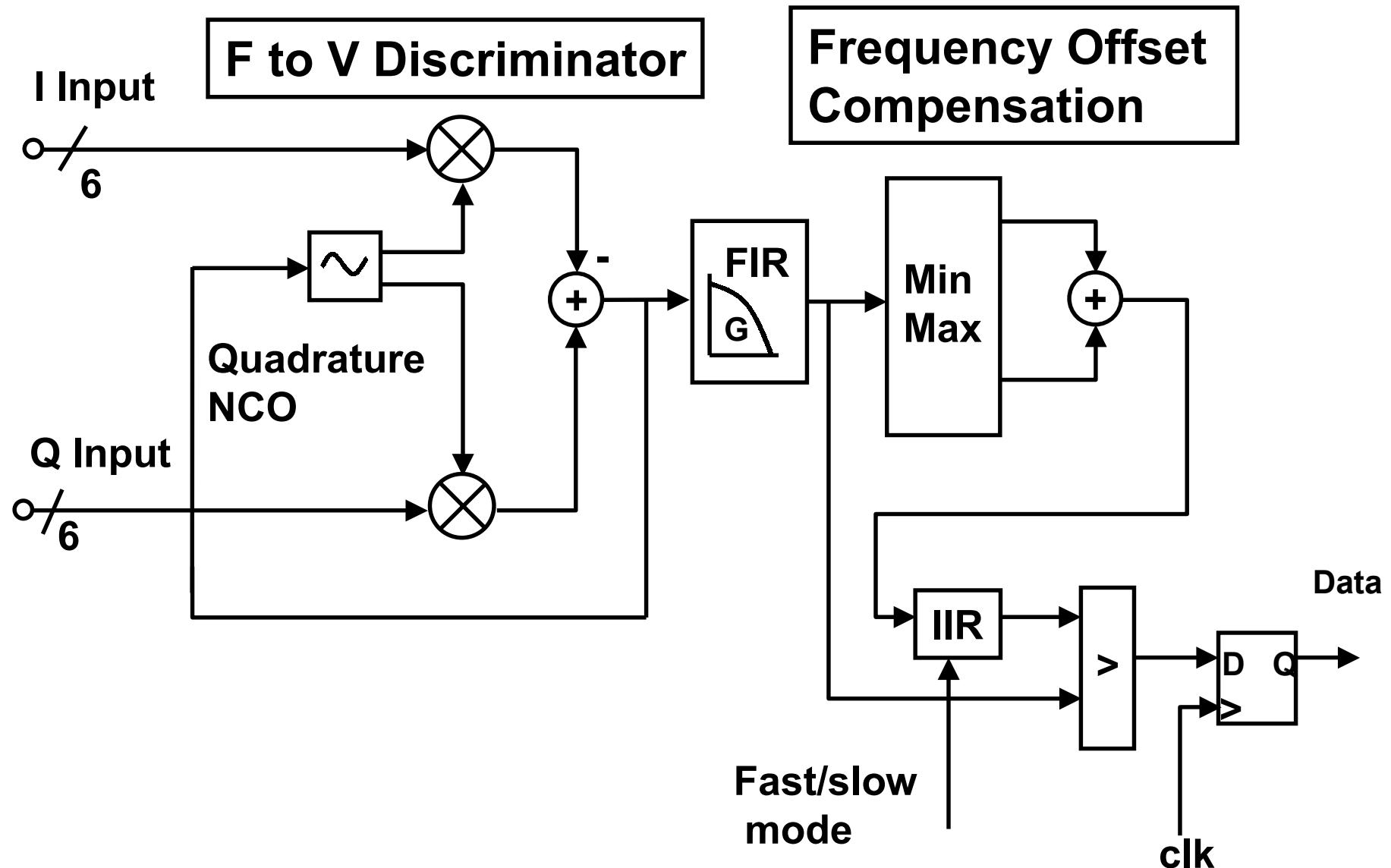
- No external components
- 7 complex poles and 5 VGA's
- Automatic tuning $\pm 200\text{kHz}$
- VGA gain: 84dB dynamic range with 1dB resolution
- AGC range 60dB

RC Oscillator Based IF Filter Tuning



$\pm 200\text{kHz}$ center frequency tuning range

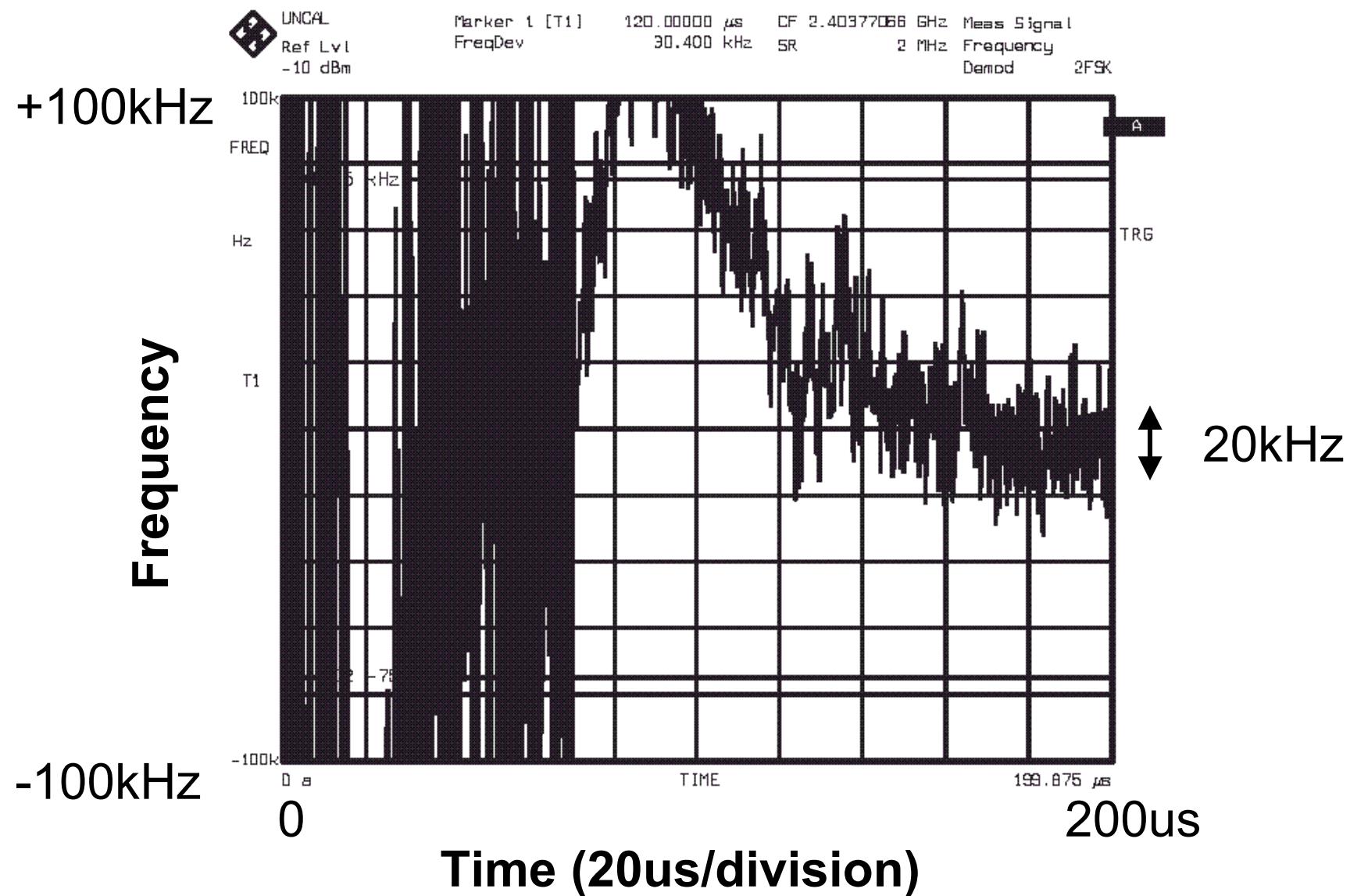
Complex PLL Demodulator



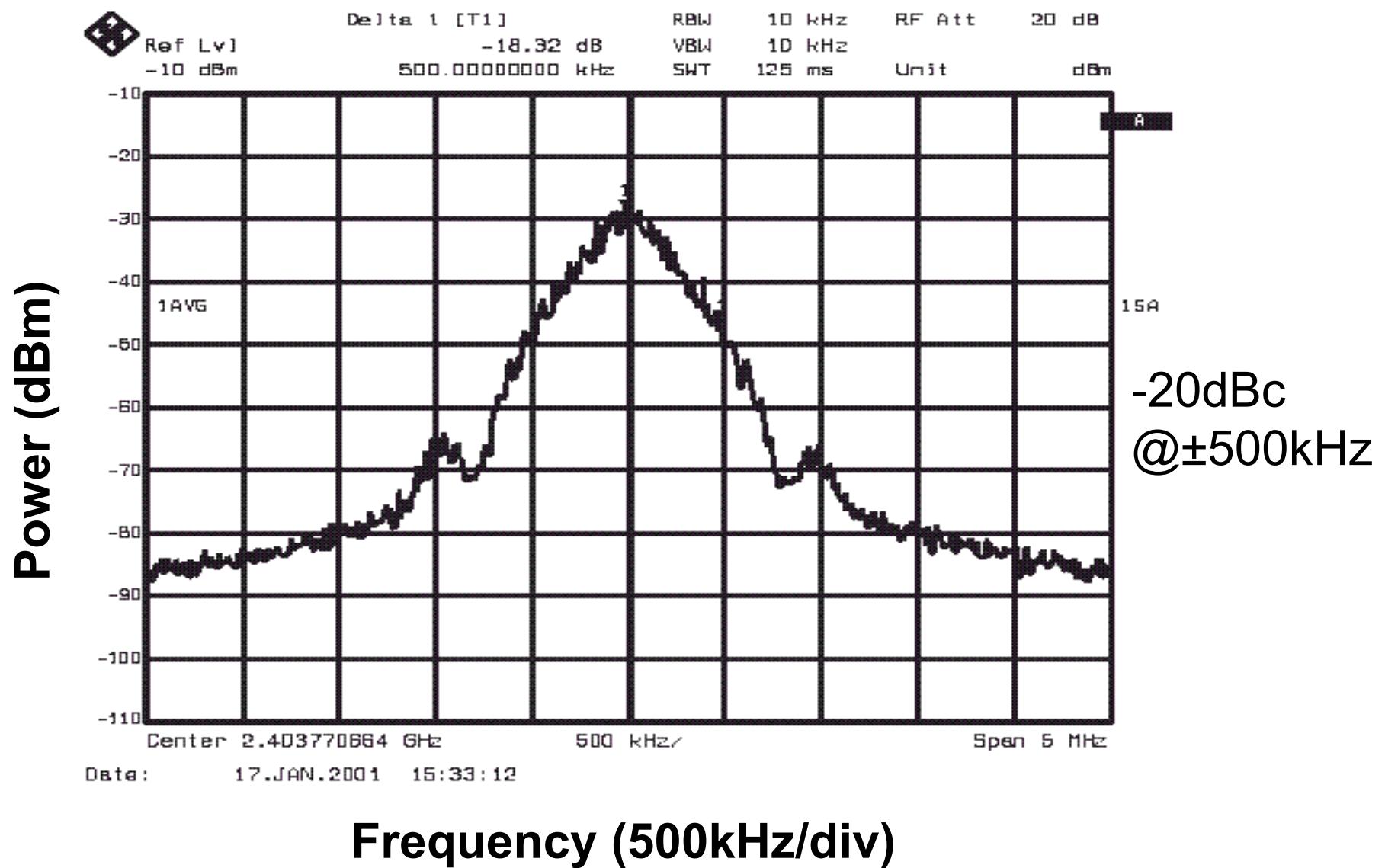
Complex PLL Advantages

- Coherent FM demodulator
- Can tolerate $\pm 325\text{kHz}$ offset
- 1st order control system
 - Unconditionally stable
 - Acquisition range = loop gain
- Acquisition time < 1 μs
- Supports 4-level GFSK demodulation

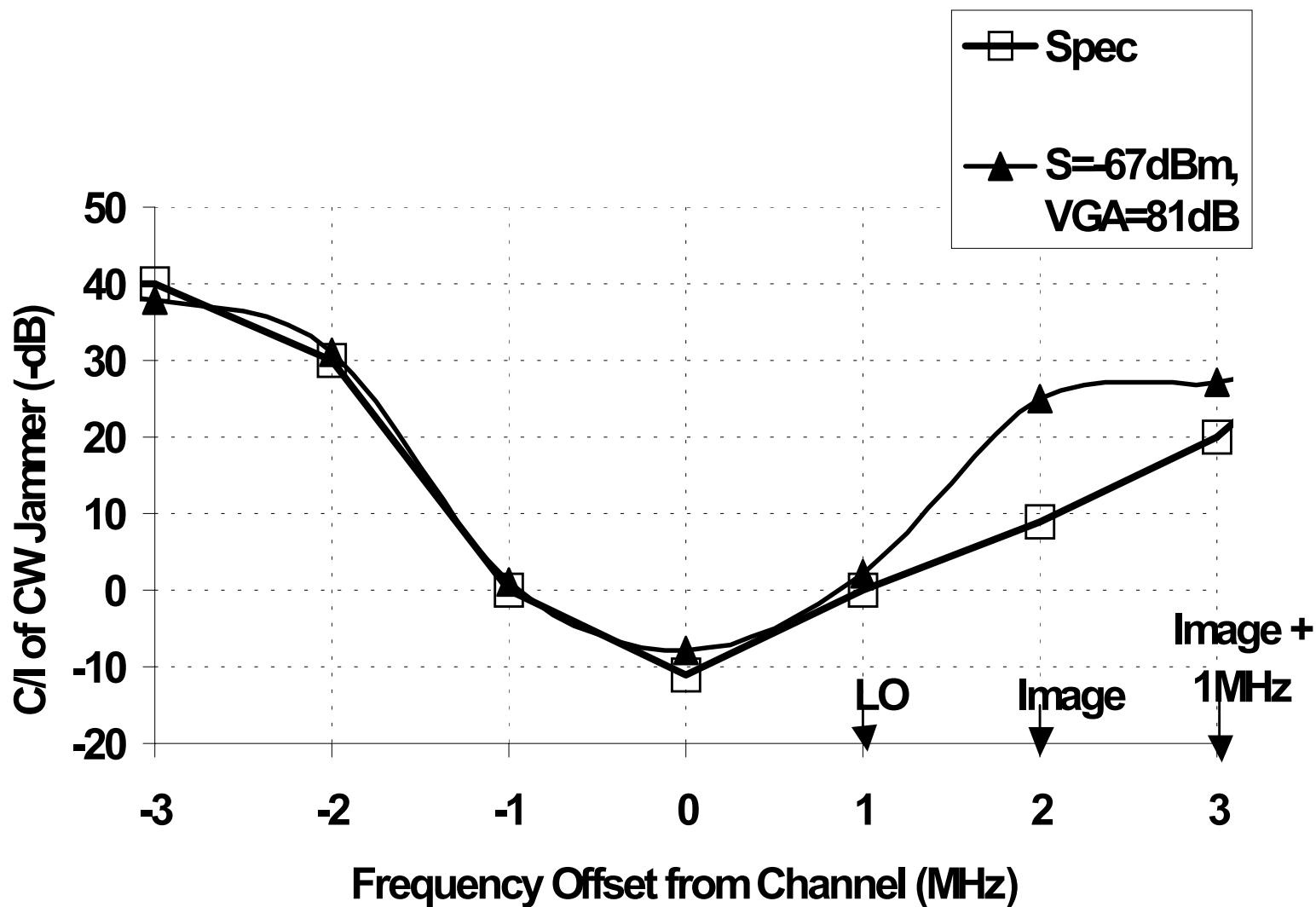
Settling Curve for 80MHz Hop



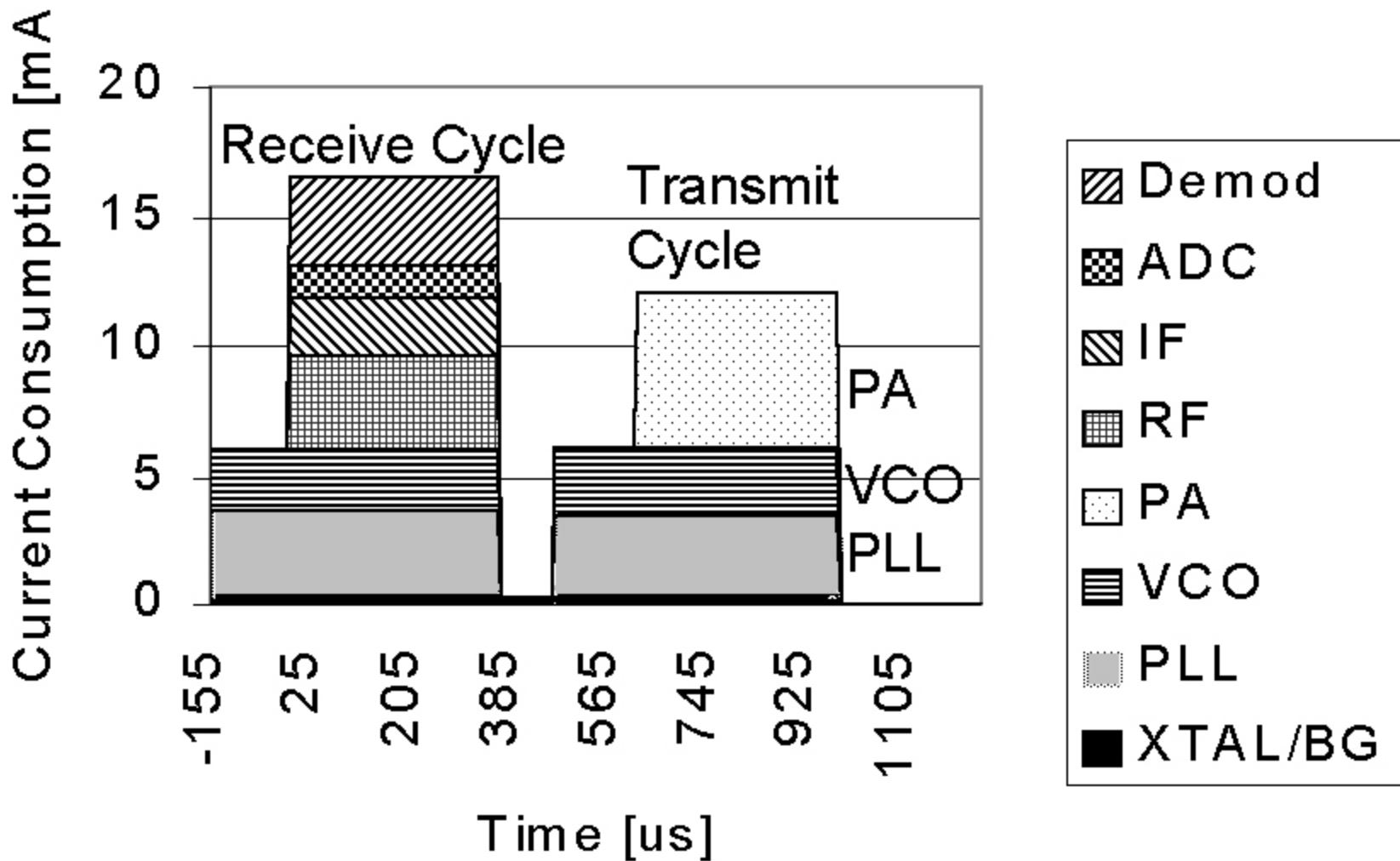
Transmit Spectral Mask



Blocker Rejection



Current Consumption by Block



Power Comparison

	Standard	Tx Power	Peak Power Consumption	Technology
J. Craninckx et al.	DECT	-6dBm	60mA@2.7V =162mW	BiCMOS
G. L. Puma et al.	DECT		50mA@3.1V =155mW	Si Bipolar
F. Op 'T Eynde et al.	Bluetooth (BB)	+2dBm	50mA@2.5V =125mW	0.25um CMOS
H. Darabi et al.	Bluetooth	+5dBm	47mA@2.7V =127mW	CMOS
This Work	Bluetooth	+2dBm	17mA@1.8V =31mW	SiGe BiCMOS

Key Performance Summary

Parameter	Bluetooth Specification	Achieved
Centre frequency	$\pm 75\text{kHz}$ (220us)	$\pm 75\text{kHz}$ (120us)
Transmit mask	-20dBc @ $\pm 550\text{kHz}$	-20dBc @ $\pm 500\text{kHz}$
Sensitivity (BER=10 ⁻³)	-70dBm	-78dBm
Co-Channel interference (C/I)	11dB	9dB
1MHz Blocker (C/I)	0dB	0dB
2MHz Blocker (C/I)	-30dB	-30dB
3MHz Blocker(C/I)	-40dB	-39dB

Conclusions

- Fully integrated Bluetooth transceiver
- Direct two-point modulation
- Complex IF filtering with on chip tuning
- 1.6V - 3.0V operation
- Average power consumption 22mW @
+2dBm Tx power

Photo Micrograph

