13.4 A 22mW Bluetooth RF Transceiver with Direct RF Modulation and On-chip IF Filtering

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The Bluetooth wireless standard defines short range (10-100m) networking between electronic devices in the unlicensed 2.4GHz ISM band [1]. The air interface specifies a 1600 hop/s spread spectrum TDD format and 1Mb/s GFSK modulation using 79 1MHz channels. Low power consumption, low cost and small form-factor are crucial for adoption by battery-constrained portable devices.

This Bluetooth RF transceiver has 22mW average power consumption at +2dBm power output. A block diagram of this transceiver is shown in Figure 13.4.1. The transmitter consists of a ΣΔ fractional-N frequency synthesizer with on-chip VCO and two-point modulation at RF. This architecture keeps the carrier locked during modulation while eliminating the use of two 2.4GHz up-conversion mixers. The receiver has a single-conversion complex I/Q low-IF architecture with integrated tunable filters, distributed AGC, and a complex-PLL (CPLL) digital demodulator. The IC is controlled by transmit and receive state machines, programmed via a serial port interface. An on-chip tunable crystal oscillator allows operation from either a 10MHz or 13MHz crystal. The complete transceiver operates from a 1.8V to 3.6V supply and requires an external PLL loop filter, balun for the receiver input and optionally for the transmitter output, an RF filter, T/R switch, and decoupling capacitors.

For transmit path, a two-point modulation scheme generates the 1Mb/s 2-GFSK. The ΣΔ fractional-N frequency synthesizer allows accurate digital control of the low-frequency modulation path, defined by the loop bandwidth. The high-frequency modulation content is generated by direct VCO modulation. A calibration circuit aligns the analog modulation constant to the well-defined digital constant. Once calibrated, digital and analog circuitry maintains the analog path within the allowed deviation tolerance. A fully-integrated VCO has a tuning range of 350MHz to cover the 2.4-2.5GHz ISM band. A plot of the tuning curve is shown in Figure 13.4.2. This VCO has 1mA current consumption and -99dBc/Hz phase noise at 100kHz. To meet settling time requirements, a speed-up circuit is used in the PLL to increase the loop bandwidth during acquisition. This achieves settling times of <120μs to within 50kHz of the channel frequency. A plot of the transmit spectral mask at 2.402GHz is shown in Figure 13.4.3. The power amplifier has a 50Ω single-ended output power range from -13dBm to +2dBm with digital control, allowing Bluetooth class-2 operation. Peak power consumption is under 18mW at -6dBm, an order of magnitude better than a recent DECT transmitter (similar modulation format and output power in 1.9GHz band) that uses a direct up-conversion architecture [2].

In the receive path, the LNA input is differential, requiring an external balun for single-ended conversion. The LNA-mixer down-converter (Figure 3.4.4) has 14dB small signal gain, 6.5dB noise figure and -15dBm IIP3. The I/Q mixers and LO signals are sufficiently balanced in amplitude and phase to provide >21dB image rejection. The LNA-mixer down-converter is capable of 1V operation while maintaining the same performance.

A low-IF receiver topology mitigates static and dynamic DC offset problems when dealing with low modulation index (MI) FSK transmission, as in Bluetooth (MI=0.28 to 0.35). IF filtering and AGC functions are in the complex domain using seven complex poles interleaved with five fixed-step variable-gain amplifiers (VGAs). The continuous-time IF filter is digitally tuned by measuring the frequency of an on-chip R-C oscillator. The complex filter response can be inferred from Figure 13.4.5, which plots blocker rejection. For each VGA, the difference between the input level and the required output level is determined, and then digital hardware in a feedforward configuration sets the gain. The input level is measured using all four phases of the I/Q signal and achieves accurate settling in <4μs, allowing the VGAs to settle during the 4μs packet preamble. The total VGA gain varies over an 84dB range with 1dB resolution. Signal strength is estimated with a weighted sum of the VGA digital gain settings. The use of an IF strip with AGC means only 6b resolution is needed in the I/Q digitizing ADCs.

Demodulation uses a digital CPLL, which provides <1ms signal acquisition response and coherent detection for improved sensitivity. The CPLL uses truncated digital multipliers, which reduce power consumption with minimal SNR impact. A Gaussian digital FIR filter performs post-demodulation filtering to improve SNR before slicing. The digital bit slicer adaptively tracks the nominal level of the demodulated signal to estimate the optimum decision threshold due to frequency drifts and offsets which can be greater than 80% of the modulation deviation. Optional 4-level GFSK demodulation is available. The receiver sensitivity is better than -78dBm at BER=0.001.

Transmit and receive state machines insure that the various transceiver blocks are powered up at appropriate times to minimize power consumption. Figure 13.4.6 illustrates the timing/current of the individual blocks as they are turned on and off in transmit/receive mode. The peak current drawn in 2.0V operation is in receive mode and is 16.4mA, with the distribution of consumption as follows: RF Front-end 24%, digital demodulator 18%, VCO 22%, IF filter and AGC 16%, PLL 11%, crystal oscillator and bias 3%.

The IC is programmed through a four-wire serial programmable interface (SPI) and two mode pins which establish transmit, receive, test and power-down states. The SPI contains 64 registers, which operate up to 4MHz. The transceiver is implemented in a 0.5μm SiGe BiCMOS process and the die is mounted in a 48-pin BCC++ package with exposed paddle. A die micrograph is shown in Figure 13.4.7.

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Op't Eynde, F. et al., "A Fully-Integrated Zero-IF DECT Transceiver", ISSCC Digest of Technical Papers, pp.138-139, Feb 2000.

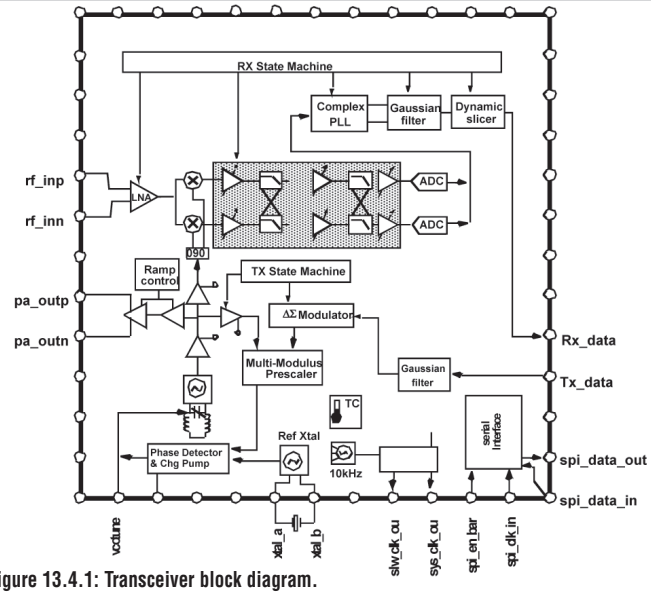

Figure 13.4.1: Transceiver block diagram.

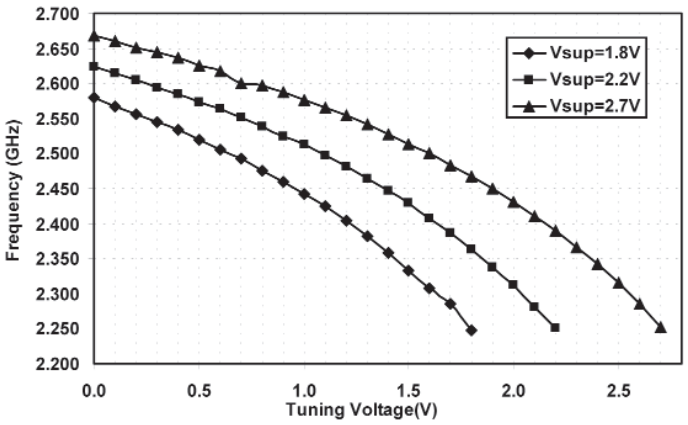

Figure 13.4.2: VCO tuning curve vs. supply voltage.

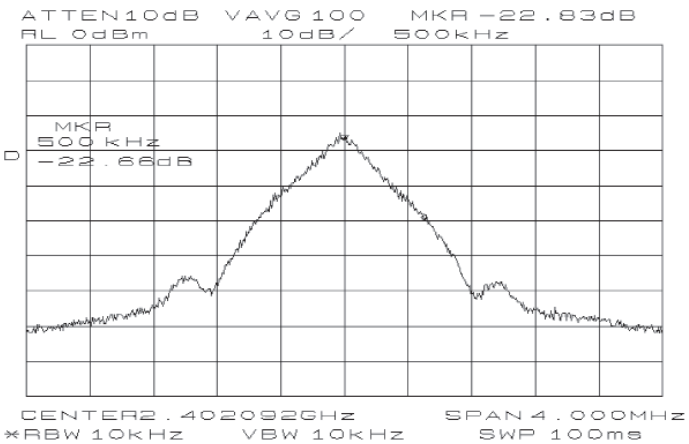

Figure 13.4.3: Transmit spectral mask, relative to a -20dBm carrier output level.

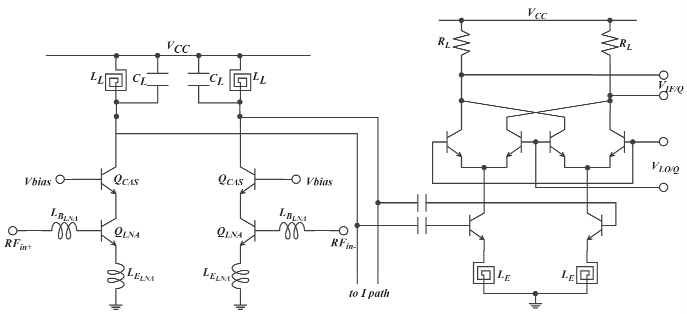

Figure 13.4.4: IV LNA/Mixer downconverter.

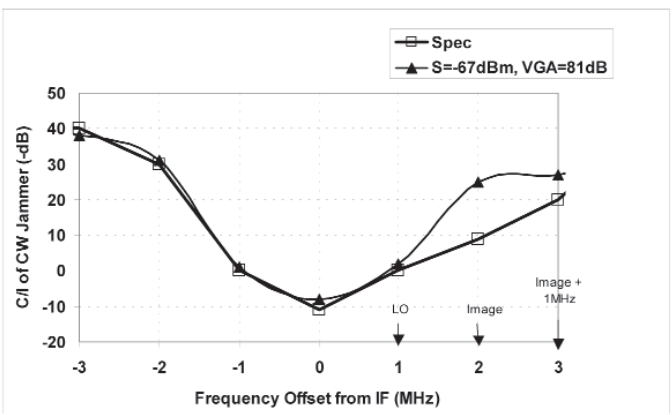

Figure 13.4.5: Blocker performance measured via desensitization power with input signal level at -67dBm.

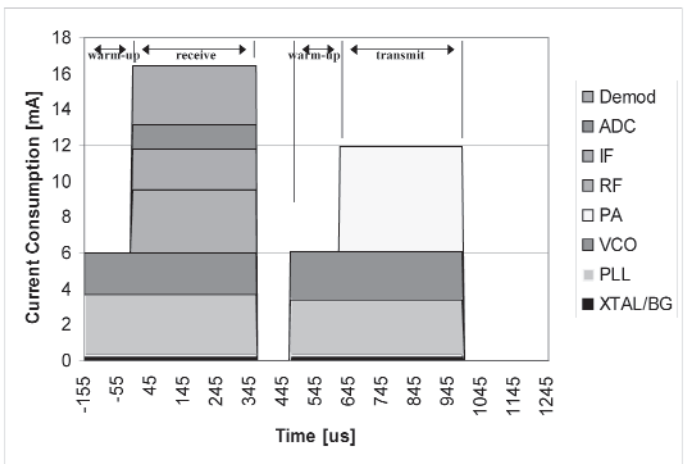

Figure 13.4.6: Measured current consumption at 2.0V, +2dBm PA output, using a 10MHz reference clock.

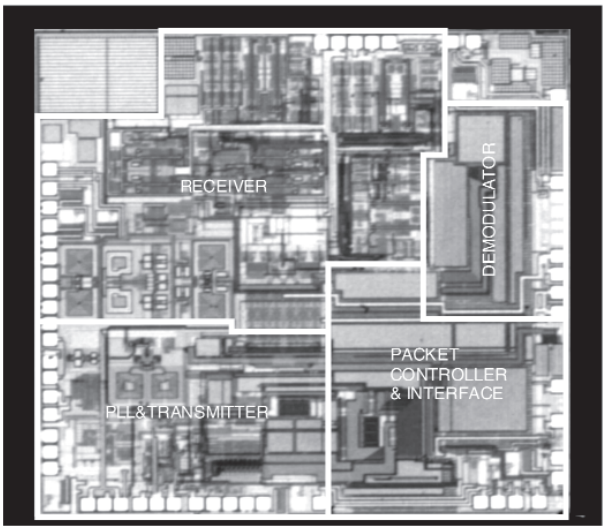

Figure 13.4.7: Die micrograph.